CLAIM AMENDMENTS

Claims 1-22 *(CANCELLED)*

23. *(NEW)* An apparatus including integrated processor circuitry, said apparatus comprising:

a plurality of interface electrodes including one or more control electrodes to convey one or more incoming control signals from at least one signal source having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode;

control circuitry coupled to said one or more control electrodes and responsive to said one or more incoming control signals by providing at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states with said respective assertion states following said first incoming control signal states combination;

clock circuitry coupled to said control circuitry and responsive to said at least one clock control signal by providing at least a first clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively; and

a plurality of subcircuits coupled to at least a portion of said plurality of interface electrodes, said control circuitry and said clock circuitry, and including pipeline subcircuitry responsive to said first clock signal by selectively operating on one or more instructions for data processing, wherein

a first portion of said pipeline subcircuitry is responsive to said active first clock signal by performing at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions to provide one or more decoded instructions, and

a second portion of said pipeline subcircuitry is coupled to said first pipeline subcircuitry portion and responsive to said active first clock signal by

executing said one or more decoded instructions.

24. *(NEW)* The apparatus of claim 23, wherein said control circuitry further provides a status signal indicative of said respective assertion states of said at least one clock control signal.

25. *(NEW)* The apparatus of claim 23, wherein said control circuitry comprises logic circuitry that converts said one or more incoming control signals to said at least one clock control signal.

26. *(NEW)* The apparatus of claim 23, wherein said control circuitry comprises at least one register in which said one or more incoming control signals is stored to provide said at least one clock control signal.

27. *(NEW)* The apparatus of claim 23, wherein said clock circuitry further provides a second clock signal with active and inactive states substantially independent of said at least one clock control signal assertion and de-assertion states.

28. *(NEW)* The apparatus of claim 23, wherein said first pipeline subcircuitry portion comprises decoding circuitry.

29. *(NEW)* The apparatus of claim 23, wherein said second pipeline subcircuitry portion comprises arithmetic logic circuitry.

30. *(NEW)* The apparatus of claim 23, wherein said control circuitry is responsive to a second combination of said one or more incoming control signal assertion and de-assertion states by providing said at least one clock control signal in said respective de-assertion states.

31. *(NEW)* The apparatus of claim 23, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

32. *(NEW)* The apparatus of claim 23, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

33. *(NEW)* The apparatus of claim 23, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

34. *(NEW)* The apparatus of claim 23, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

35. *(NEW)* The apparatus of claim 23, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having

respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

36. *(NEW)* The apparatus of claim 23, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

37. *(NEW)* The apparatus of claim 23, wherein said control circuitry provides said at least one clock control signal in said respective assertion states following:

said first combination of said one or more incoming control signal assertion and de-assertion states; and

completion of

said performance, initiated prior to said first combination of said one or more incoming control signal assertion and de-assertion states, by said first pipeline subcircuitry portion of said at least one or more respective portions of said one or more decoding operations to provide said one or more decoded instructions, and

said execution by said second pipeline subcircuitry portion of said one or more decoded instructions.

38. *(NEW)* The apparatus of claim 37, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

39. *(NEW)* The apparatus of claim 37, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

40. *(NEW)* The apparatus of claim 37, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

41. *(NEW)* The apparatus of claim 37, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

42. *(NEW)* The apparatus of claim 37, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

43. *(NEW)* The apparatus of claim 37, wherein said plurality of subcircuits

further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

44. *(NEW)* An apparatus including integrated processor circuitry, said apparatus comprising:

interface means for conveying one or more incoming control signals from at least one signal source having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode;

controller means for responding to said one or more incoming control signals by generating at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states with said respective assertion states following said first incoming control signal states combination;

clock source means for responding to said at least one clock control signal by generating at least a first clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively; and

subcircuit means including pipeline means for responding to said first clock signal by selectively operating on one or more instructions for data processing, wherein

a first portion of said pipeline means is for responding to said active first clock signal by performing at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions to provide one or more decoded instructions, and

a second portion of said pipeline means is for responding to said active first clock signal by executing said one or more decoded instructions.

45. *(NEW)* An apparatus including integrated processor circuitry, said apparatus comprising:

a plurality of interface electrodes including one or more control electrodes to convey one or more incoming control signals from at least one signal source having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode;

control circuitry coupled to said one or more control electrodes and responsive to said one or more incoming control signals by providing at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states;

clock circuitry coupled to said control circuitry and responsive to said at least one clock control signal by providing at least a first clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively, with said inactive state following said first incoming control signal states combination; and

a plurality of subcircuits coupled to at least a portion of said plurality of interface electrodes, said control circuitry and said clock circuitry, and including pipeline subcircuitry responsive to said first clock signal by selectively operating on one or more instructions for data processing, wherein

a first portion of said pipeline subcircuitry is responsive to said active first clock signal by performing at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions to provide one or more decoded instructions, and

a second portion of said pipeline subcircuitry is coupled to said first pipeline subcircuitry portion and responsive to said active first clock signal by executing said one or more decoded instructions.

46. *(NEW)* The apparatus of claim 45, wherein said control circuitry

further provides a status signal indicative of said first clock signal inactive state.

47. *(NEW)* The apparatus of claim 45, wherein said control circuitry comprises logic circuitry that converts said one or more incoming control signals to said at least one clock control signal.

48. *(NEW)* The apparatus of claim 45, wherein said control circuitry comprises at least one register in which said one or more incoming control signals is stored to provide said at least one clock control signal.

49. *(NEW)* The apparatus of claim 45, wherein said clock circuitry further provides a second clock signal with active and inactive states substantially independent of said at least one clock control signal assertion and de-assertion states.

50. *(NEW)* The apparatus of claim 45, wherein said first pipeline subcircuitry portion comprises decoding circuitry.

51. *(NEW)* The apparatus of claim 45, wherein said second pipeline subcircuitry portion comprises arithmetic logic circuitry.

52. *(NEW)* The apparatus of claim 45, wherein said control and clock circuitries together are responsive to a second combination of said one or more incoming control signal assertion and de-assertion states by providing said first clock signal in said active state.

53. *(NEW)* The apparatus of claim 45, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said

control circuitry to said one or more incoming control signals.

54. *(NEW)* The apparatus of claim 45, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

55. *(NEW)* The apparatus of claim 45, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

56. *(NEW)* The apparatus of claim 45, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

57. *(NEW)* The apparatus of claim 45, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

58. *(NEW)* The apparatus of claim 45, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

59. *(NEW)* The apparatus of claim 45, wherein said clock circuitry provides said first clock signal in said inactive state following:

said first combination of said one or more incoming control signal assertion and de-assertion states; and

completion of

said performance, initiated prior to said first combination of said one or more incoming control signal assertion and de-assertion states, by said first pipeline subcircuitry portion of said at least one or more respective portions of said one or more decoding operations to provide said one or more decoded instructions, and

said execution by said second pipeline subcircuitry portion of said one or more decoded instructions.

60. *(NEW)* The apparatus of claim 59, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

61. *(NEW)* The apparatus of claim 59, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said

clock circuitry to said at least one clock control signal.

62. *(NEW)* The apparatus of claim 59, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

63. *(NEW)* The apparatus of claim 59, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

64. *(NEW)* The apparatus of claim 59, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

65. *(NEW)* The apparatus of claim 59, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

66. *(NEW)* An apparatus including integrated processor circuitry, said apparatus comprising:

interface means for conveying one or more incoming control signals from at least one signal source having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode;

controller means for responding to said one or more incoming control signals by generating at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states;

clock source means for responding to said at least one clock control signal by generating at least a first clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively, with said inactive state following said first incoming control signal states combination; and

subcircuit means including pipeline means for responding to said first clock signal by selectively operating on one or more instructions for data processing, wherein

a first portion of said pipeline means is for responding to said active first clock signal by performing at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions to provide one or more decoded instructions, and

a second portion of said pipeline means is for responding to said active first clock signal by executing said one or more decoded instructions.

67. *(NEW)* An apparatus including integrated processor circuitry, said apparatus comprising:

a plurality of interface electrodes including one or more control electrodes to convey one or more incoming control signals from at least one signal source having at

least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode;

control circuitry coupled to said one or more control electrodes and responsive to said one or more incoming control signals by providing at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states with said respective assertion states following said first incoming control signal states combination;

clock circuitry coupled to said control circuitry and responsive to said at least one clock control signal by providing at least a first clock signal having an active state having a plurality of successive cycles and an inactive state having substantially zero cycles corresponding to said at least one clock control signal de-assertion and assertion states, respectively; and

a plurality of subcircuits coupled to at least a portion of said plurality of interface electrodes, said control circuitry and said clock circuitry, and including pipeline subcircuitry responsive to said first clock signal by selectively operating on one or more instructions for data processing, wherein

a first portion of said pipeline subcircuitry is responsive to at least a first one of said plurality of first clock signal cycles by performing at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions to provide one or more decoded instructions, and

a second portion of said pipeline subcircuitry is coupled to said first pipeline subcircuitry portion and responsive to at least a second one subsequent to said first one of said plurality of first clock signal cycles by executing said one or more decoded instructions.

68. *(NEW)* The apparatus of claim 67, wherein said control circuitry further provides a status signal indicative of said respective assertion states of said at least one clock control signal.

69. *(NEW)* The apparatus of claim 67, wherein said control circuitry comprises logic circuitry that converts said one or more incoming control signals to said at least one clock control signal.

70. *(NEW)* The apparatus of claim 67, wherein said control circuitry comprises at least one register in which said one or more incoming control signals is stored to provide said at least one clock control signal.

71. *(NEW)* The apparatus of claim 67, wherein said clock circuitry further provides a second clock signal with active and inactive states substantially independent of said at least one clock control signal assertion and de-assertion states.

72. *(NEW)* The apparatus of claim 67, wherein said first pipeline subcircuitry portion comprises decoding circuitry.

73. *(NEW)* The apparatus of claim 67, wherein said second pipeline subcircuitry portion comprises arithmetic logic circuitry.

74. *(NEW)* The apparatus of claim 67, wherein said control circuitry is responsive to a second combination of said one or more incoming control signal assertion and de-assertion states by providing said at least one clock control signal in said respective de-assertion states.

75. *(NEW)* The apparatus of claim 67, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

76. *(NEW)* The apparatus of claim 67, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

77. *(NEW)* The apparatus of claim 67, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

78. *(NEW)* The apparatus of claim 67, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

79. *(NEW)* The apparatus of claim 67, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

80. *(NEW)* The apparatus of claim 67, wherein said plurality of subcircuits

further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

81. *(NEW)* The apparatus of claim 67, wherein said control circuitry provides said at least one clock control signal in said respective assertion states following:

said first combination of said one or more incoming control signal assertion and de-assertion states; and

completion of

said performance, initiated prior to said first combination of said one or more incoming control signal assertion and de-assertion states, by said first pipeline subcircuitry portion of said at least one or more respective portions of said one or more decoding operations to provide said one or more decoded instructions, and

said execution by said second pipeline subcircuitry portion of said one or more decoded instructions.

82. *(NEW)* The apparatus of claim 81, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

83. *(NEW)* The apparatus of claim 81, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said

clock circuitry to said at least one clock control signal.

84. *(NEW)* The apparatus of claim 81, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

85. *(NEW)* The apparatus of claim 81, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

86. *(NEW)* The apparatus of claim 81, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

87. *(NEW)* The apparatus of claim 81, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

88. *(NEW)* An apparatus including integrated processor circuitry, said apparatus comprising:

interface means for conveying one or more incoming control signals from at least one signal source having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode;

controller means for responding to said one or more incoming control signals by generating at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states with said respective assertion states following said first incoming control signal states combination;

clock source means for responding to said at least one clock control signal by generating at least a first clock signal having an active state having a plurality of successive cycles and an inactive state having substantially zero cycles corresponding to said at least one clock control signal de-assertion and assertion states, respectively; and

subcircuit means including pipeline means for responding to said first clock signal by selectively operating on one or more instructions for data processing, wherein

a first portion of said pipeline means is for responding to at least a first one of said plurality of first clock signal cycles by performing at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions to provide one or more decoded instructions, and

a second portion of said pipeline means is for responding to at least a second one subsequent to said first one of said plurality of first clock signal cycles by executing said one or more decoded instructions.

89. *(NEW)* An apparatus including integrated processor circuitry, said

apparatus comprising:

a plurality of interface electrodes including one or more control electrodes to convey one or more incoming control signals from at least one signal source having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode;

control circuitry coupled to said one or more control electrodes and responsive to said one or more incoming control signals by providing at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states;

clock circuitry coupled to said control circuitry and responsive to said at least one clock control signal by providing at least a first clock signal with an active state having a plurality of successive cycles and an inactive state having substantially zero cycles corresponding to said at least one clock control signal de-assertion and assertion states, respectively, with said inactive state following said first incoming control signal states combination; and

a plurality of subcircuits coupled to at least a portion of said plurality of interface electrodes, said control circuitry and said clock circuitry, and including pipeline subcircuitry responsive to said first clock signal by selectively operating on one or more instructions for data processing, wherein

a first portion of said pipeline subcircuitry is responsive to at least a first one of said plurality of first clock signal cycles by performing at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions to provide one or more decoded instructions, and

a second portion of said pipeline subcircuitry is coupled to said first pipeline subcircuitry portion and responsive to at least a second one subsequent to said first one of said plurality of first clock signal cycles by executing said one or more decoded instructions.

90. *(NEW)* The apparatus of claim 89, wherein said control circuitry further provides a status signal indicative of said first clock signal inactive state.

91. *(NEW)* The apparatus of claim 89, wherein said control circuitry comprises logic circuitry that converts said one or more incoming control signals to said at least one clock control signal.

92. *(NEW)* The apparatus of claim 89, wherein said control circuitry comprises at least one register in which said one or more incoming control signals is stored to provide said at least one clock control signal.

93. *(NEW)* The apparatus of claim 89, wherein said clock circuitry further provides a second clock signal with active and inactive states substantially independent of said at least one clock control signal assertion and de-assertion states.

94. *(NEW)* The apparatus of claim 89, wherein said first pipeline subcircuitry portion comprises decoding circuitry.

95. *(NEW)* The apparatus of claim 89, wherein said second pipeline subcircuitry portion comprises arithmetic logic circuitry.

96. *(NEW)* The apparatus of claim 89, wherein said control and clock circuitries together are responsive to a second combination of said one or more incoming control signal assertion and de-assertion states by providing said first clock signal in said active state.

97. *(NEW)* The apparatus of claim 89, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said

execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

98. *(NEW)* The apparatus of claim 89, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

99. *(NEW)* The apparatus of claim 89, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

100. *(NEW)* The apparatus of claim 89, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

101. *(NEW)* The apparatus of claim 89, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

102. *(NEW)* The apparatus of claim 89, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

103. *(NEW)* The apparatus of claim 89, wherein said clock circuitry provides said first clock signal in said inactive state following:

said first combination of said one or more incoming control signal assertion and de-assertion states; and

completion of

said performance, initiated prior to said first combination of said one or more incoming control signal assertion and de-assertion states, by said first pipeline subcircuitry portion of said at least one or more respective portions of said one or more decoding operations to provide said one or more decoded instructions, and

said execution by said second pipeline subcircuitry portion of said one or more decoded instructions.

104. *(NEW)* The apparatus of claim 103, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

105. *(NEW)* The apparatus of claim 103, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states

determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

106. *(NEW)* The apparatus of claim 103, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

107. *(NEW)* The apparatus of claim 103, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

108. *(NEW)* The apparatus of claim 103, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

109. *(NEW)* The apparatus of claim 103, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least

one clock control signal.

110. *(NEW)* An apparatus including integrated processor circuitry, said apparatus comprising:

interface means for conveying one or more incoming control signals from at least one signal source having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode;

controller means for responding to said one or more incoming control signals by generating at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states;

clock source means for responding to said at least one clock control signal by generating at least a first clock signal with an active state having a plurality of successive cycles and an inactive state having substantially zero cycles corresponding to said at least one clock control signal de-assertion and assertion states, respectively, with said inactive state following said first incoming control signal states combination; and

subcircuit means including pipeline means for responding to said first clock signal by selectively operating on one or more instructions for data processing, wherein

a first portion of said pipeline means is for responding to at least a first one of said plurality of first clock signal cycles by performing at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions to provide one or more decoded instructions, and

a second portion of said pipeline means is for responding to at least a second one subsequent to said first one of said plurality of first clock signal cycles by executing said one or more decoded instructions.

111. *(NEW)* An apparatus including integrated processor circuitry, said apparatus comprising:

a plurality of interface electrodes including one or more control electrodes to convey one or more incoming control signals from at least one signal source having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode;

control circuitry coupled to said one or more control electrodes and responsive to said one or more incoming control signals and a first clock signal by providing at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states with said respective assertion states following said first incoming control signal states combination;

clock circuitry coupled to said control circuitry and responsive to said at least one clock control signal by providing said first clock signal having active and inactive states substantially independent of said at least one clock control signal assertion and de-assertion states, and a second clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively; and

a plurality of subcircuits coupled to at least a portion of said plurality of interface electrodes, said control circuitry and said clock circuitry, and including pipeline subcircuitry responsive to said active second clock signal by executing one or more instructions for data processing.

112. *(NEW)* The apparatus of claim 111, wherein said control circuitry further provides a status signal indicative of said respective assertion states of said at least one clock control signal.

113. *(NEW)* The apparatus of claim 111, wherein said control circuitry comprises logic circuitry that converts said one or more incoming control signals to

said at least one clock control signal.

114. *(NEW)* The apparatus of claim 111, wherein said control circuitry comprises at least one register in which said one or more incoming control signals is stored to provide said at least one clock control signal.

115. *(NEW)* The apparatus of claim 111, wherein said pipeline subcircuitry comprises decoding circuitry.

116. *(NEW)* The apparatus of claim 111, wherein said pipeline subcircuitry comprises arithmetic logic circuitry.

117. *(NEW)* The apparatus of claim 111, wherein said control circuitry is responsive to a second combination of said one or more incoming control signal assertion and de-assertion states by providing said at least one clock control signal in said respective de-assertion states.

118. *(NEW)* The apparatus of claim 111, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said second clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

119. *(NEW)* The apparatus of claim 111, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said second clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

120. *(NEW)* The apparatus of claim 111, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said second clock signal by retaining, until a reactivation of said second clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

121. *(NEW)* The apparatus of claim 111, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said second clock signal by retaining, until a reactivation of said second clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

122. *(NEW)* The apparatus of claim 111, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said second clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

123. *(NEW)* The apparatus of claim 111, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said second clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

124. *(NEW)* The apparatus of claim 111, wherein said control circuitry

provides said at least one clock control signal in said respective assertion states following:

said first combination of said one or more incoming control signal assertion and de-assertion states; and

completion of said execution of said one or more instructions for data processing initiated prior to said first combination of said one or more incoming control signal assertion and de-assertion states.

125. *(NEW)* The apparatus of claim 124, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said second clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

126. *(NEW)* The apparatus of claim 124, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said second clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

127. *(NEW)* The apparatus of claim 124, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said second clock signal by retaining, until a reactivation of said second clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

128. *(NEW)* The apparatus of claim 124, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said

second clock signal by retaining, until a reactivation of said second clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

129. *(NEW)* The apparatus of claim 124, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said second clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

130. *(NEW)* The apparatus of claim 124, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said second clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

131. *(NEW)* An apparatus including integrated processor circuitry, said apparatus comprising:

interface means for conveying one or more incoming control signals from at least one signal source having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode;

controller means for responding to said one or more incoming control signals and a first clock signal by generating at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states with said respective assertion states following said first incoming control signal states combination;

clock source means for responding to said at least one clock control signal by generating said first clock signal having active and inactive states substantially independent of said at least one clock control signal assertion and de-assertion states, and a second clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively; and

subcircuit means including pipeline means for responding to said active second clock signal by executing one or more instructions for data processing.

132. *(NEW)* An apparatus including integrated processor circuitry, said apparatus comprising:

a plurality of interface electrodes including one or more control electrodes to convey one or more incoming control signals from at least one signal source having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode;

control circuitry coupled to said one or more control electrodes and responsive to said one or more incoming control signals and a first clock signal by providing at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states;

clock circuitry coupled to said control circuitry and responsive to said at least one clock control signal by providing said first clock signal having active and inactive states substantially independent of said at least one clock control signal assertion and de-assertion states, and a second clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively, with said second clock signal inactive state following said first incoming control signal states combination; and

a plurality of subcircuits coupled to at least a portion of said plurality of interface electrodes, said control circuitry and said clock circuitry, and including pipeline subcircuitry responsive to said active second clock signal by executing one or more instructions for data processing.

133. *(NEW)* The apparatus of claim 132, wherein said control circuitry further provides a status signal indicative of said second clock signal inactive state.

134. *(NEW)* The apparatus of claim 132, wherein said control circuitry comprises logic circuitry that converts said one or more incoming control signals to said at least one clock control signal.

135. *(NEW)* The apparatus of claim 132, wherein said control circuitry comprises at least one register in which said one or more incoming control signals is stored to provide said at least one clock control signal.

136. *(NEW)* The apparatus of claim 132, wherein said pipeline subcircuitry comprises decoding circuitry.

137. *(NEW)* The apparatus of claim 132, wherein said pipeline subcircuitry comprises arithmetic logic circuitry.

138. *(NEW)* The apparatus of claim 132, wherein said control and clock circuitries together are responsive to a second combination of said one or more incoming control signal assertion and de-assertion states by providing said second clock signal in said active state.

139. *(NEW)* The apparatus of claim 132, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said second clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

140. *(NEW)* The apparatus of claim 132, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said second clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

141. *(NEW)* The apparatus of claim 132, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said second clock signal by retaining, until a reactivation of said second clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

142. *(NEW)* The apparatus of claim 132, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said second clock signal by retaining, until a reactivation of said second clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

143. *(NEW)* The apparatus of claim 132, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said second clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

144. *(NEW)* The apparatus of claim 132, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation

following a deactivation of said second clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

145. *(NEW)* The apparatus of claim 132, wherein said clock circuitry provides said first and second clock signals in said active and inactive states, respectively, following:

said first combination of said one or more incoming control signal assertion and de-assertion states; and

completion of said execution of said one or more instructions for data processing initiated prior to said first combination of said one or more incoming control signal assertion and de-assertion states.

146. *(NEW)* The apparatus of claim 145, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said second clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

147. *(NEW)* The apparatus of claim 145, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said second clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

148. *(NEW)* The apparatus of claim 145, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said second clock signal by retaining, until a reactivation of said second clock signal, a

plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

149. *(NEW)* The apparatus of claim 145, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said second clock signal by retaining, until a reactivation of said second clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

150. *(NEW)* The apparatus of claim 145, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said second clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more incoming control signals.

151. *(NEW)* The apparatus of claim 145, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said second clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said at least one clock control signal.

152. *(NEW)* An apparatus including integrated processor circuitry, said apparatus comprising:

interface means for conveying one or more incoming control signals from at least one signal source having at least a first combination of respective assertion and

de-assertion states corresponding to a power management operation mode;

controller means for responding to said one or more incoming control signals and a first clock signal by providing at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states;

clock source means for responding to said at least one clock control signal by generating said first clock signal having active and inactive states substantially independent of said at least one clock control signal assertion and de-assertion states, and a second clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively, with said second clock signal inactive state following said first incoming control signal states combination; and

subcircuit means including pipeline means for responding to said active second clock signal by executing one or more instructions for data processing.